UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,987,690 B2
APPLICATION NO. : 10/691513
DATED : January 17, 2006
INVENTOR(S) : Hideto Hidaka

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Under "What is claimed is:", add (old claims 34 – 44) re-numbered claims 25 – 35 as followed:

Col. 43 Line 1-12

25. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and

a magnetization direction of each said magnetic storage portion in an initial state is the same as that of each said program cell in a non-program state.

Under "What is claimed is:", add

Col. 44 Line 13-26

26. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing

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Col. 44 Line 13-26 (cont'd)

data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

the magnetization directions of each said magnetic storage portion and each said program cell are respectively set along an easy axis specific to said program cell, and

said magnetic storage portion and said program cell are arranged so that said respective easy axis thereof extend in a same direction.

Under "What is claimed is:", add

Col. 44 Line 26-43

27. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

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Col. 44 Line 26-43 (cont'd)

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

each said magnetic storage portion and each said program cell include

a first magnetic layer magnetized in a fixed direction,

a second magnetic layer magnetized either in a same direction as, or in an opposite direction to, that of said first magnetic layer depending on storage data, and

an insulating film formed between said first and second magnetic layers, and

in each said program cell in said non program state and each said magnetic storage portion in said initial state, said first and second magnetic layers are magnetized in a same direction.

Under "What is claimed is:", add

Col. 44 Line 43-46

28. The thin film magnetic memory device according to claim 36, wherein a step of magnetizing said magnetic storage portions to said initial state and a step of said magnetizing each program cells to said non-program state are conducted simultaneously.

Col. 44 Line 47-65

29. A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

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Col. 44 Line 47-65 (cont'd)

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

said memory array further includes

redundant circuits provided respectively corresponding to prescribed blocks of said plurality of memory cells, each for replacing the prescribed block including a defective memory cell, and

said information stored in said program circuit includes a defective address for specifying the prescribed block including said defective memory cell,

said thin film magnetic memory device further comprising:

a redundant control circuit for controlling access to said redundant circuits based on a comparison result between an address signal for selecting said prescribed blocks and said defective address stored in said program circuit.

Under "What is claimed is:", add

Col. 45 Line 1-3

30. The thin film magnetic memory device according to claim 38, wherein

when said defective address is selected by said address signal, said redundant control circuit provides an instruction to access said redundant circuits and an instruction to discontinue access to a prescribed block corresponding to said address signal.

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Col. 45 Line 4-6

31. The thin film magnetic memory device according to claim 38, further comprising:

a monitor terminal for outputting an electric signal according to said comparison result in said redundant control circuit.

Col. 45 Line 7-12

32. A thin film magnetic memory device, comprising: a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a bias voltage applied to each said program cell in program data read operation from said program cell is lower than a voltage applied to each said magnetic storage portion in normal data read operation.

Under "What is claimed is:", add

Col. 45 Line 13-25

33. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

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Col. 45 Line 13-25(cont'd)

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of

data read operation and data write operation from and to said plurality of

memory cells, wherein

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a period during which a bias voltage is applied to each said program cell in program data read operation from said program cell is shorter than that during which a voltage is applied to each said magnetic storage portion in normal data read operation.

Under "What is claimed is:", add

Col. 45 Line 26-38

34. A thin film magnetic memory device, comprising:

a memory array having a plurality of memory cells arranged in a matrix, for magnetically storing data, wherein

each of said memory cells has a magnetic storage portion for storing data when being magnetized in one of two directions,

said thin film magnetic memory device further comprising:

a program circuit for storing information for use in at least one of data read operation and data write operation from and to said plurality of memory cells, wherein

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Col. 45 Line 26-38 (cont'd)

said program circuit includes a plurality of program units for storing program data of said information when the program unit is in a program state,

storage portion in normal data read operation.

each of said program units includes at least one program cell that is magnetized for data writing, and wherein

a voltage supplied to each said program cell in program data operation by a physical breakdown operation is higher than a voltage applied to each said magnetic storage portion in normal data read operation.

Under "What is claimed is:", add

Col. 45 Line 38-48

35. A semiconductor memory device, comprising:

a first memory including normal memory cells for storing data therein;

an address decoder coupled to said first memory and selecting the normal memory cells according to the address provided to the semiconductor memory device; and

a redundant controller coupled to said address decoder and including a second memory for storing addresses of the defective normal memory cells of said first memory, wherein said second memory has a magneto-resistance element;

said semiconductor memory device further comprises

a third memory including spare memory cells for repairing the defective normal memory cells; and

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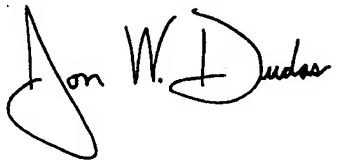
Col. 45 Line 38-48 (cont'd)

a redundant address decoder coupled to said redundant controller and said third memory, and selecting the spare memory cells according to the address stored in said second memory.

Signed and Sealed this

Thirty-first Day of July, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office